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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TABONE JR, JOHN J	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 08/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/943,895	HAN, SUNG-CHUL	
	Examiner	Art Unit	
	John J. Tabone, Jr.	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5, 7 and 9-12* is/are rejected.

7)☐ Claim(s) *6 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on *31 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07112003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-12 have been examined.

Specification

2. The disclosure is objected to because of the following informalities:

The word rectangular is incorrectly split between two lines on page 2, lines 10 and 11 and does not have a hyphen. Appropriate correction is required.

Claim Objections

3. Claims 1 and 3 are objected to because of the following informalities:

Claim 1:

The claim limitation "an UMTS," on line 1 is incorrectly used. With the first use of an acronym the meaning should accompany the acronym. Also "an" is incorrectly used. The limitation should read "a Universal Mobile Telecommunication System (UMTS). Appropriate correction is required.

Claim 3:

The claim limitation on line 2, "register updates and register parameters used to calculate..., and provides..." should read "register updates and register parameters are used to calculate..., and provides...". Appropriate correction is required.

4. Claims 6 and 8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 10-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 10:

This claim recites the claim limitation "generating an inter-row permutation pattern a(j)", however, throughout the specification a(j) is referred to as an intra-row permutation. This renders this claim vague and indefinite. Appropriate correction is required.

Claims 11 and 12:

These claims are also rejected because they depend on claim 10 and have the same problems of indefiniteness.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-3, 5, 9, and 10-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee et al. (US-6289486), hereinafter Lee.

Claim 1:

Lee teaches a register 511 stores a frame size signal and an interleaver type signal received from a system controller, as well as, a diagonal interleaving table 513 stores the numbers M and N of columns and rows in a matrix allowing optimum diagonal interleaving characteristics with respect to frame size during diagonal interleaving. (a register for updating and registering a plurality of parameters). Lee also teaches a diagonal interleaving controller 517 (address generator for generating a finally interleaved address) receives the MxN value from the diagonal interleaving table 513 and generates a read address for interleaving the information bits in a designated interleaving method. Lee further teaches a memory 523 (data storage device) receives the information bits sequentially and outputs the information bits stored at the read address received from the multiplexer 521 in an interleaved order. (Col. 5, lines 12-46, Fig. 7).

Claim 10:

Lee teaches a diagonal interleaving controller 517 receives the MxN value from the diagonal interleaving table 513 and generates a read address for interleaving the

information bits in a designated interleaving method. Lee further teaches a memory 523 (data storage device) receives the information bits sequentially and outputs the information bits stored at the read address received from the multiplexer 521 in an interleaved order (calculating a read address). (Col. 5, lines 22-25, 42-46). Lee also teaches second and third diagonal interleavings include a process for permuting an input information bit sequence (permuting an inter-row address of input data ...) expressed in an MxN matrix and enable input data to be interleaved (calculating an intra-row permutation pattern using the increment incr(j)...) . Lee further teaches diagonal interleaving addresses are operated by:

*for (j=0; j<M; j++) for (i=0; i<N, i++) new addr[i+j+N]=i+(M-1-(i+j) mod M)*N (2)*

where and i and j increment frame location (calculating and increment incr(j)) and in the third diagonal interleaving, the diagonal interleaving controller 517 can be implemented by:

*for (j=0; j<M; j++) for (i=0; i<N; i++) new addr[i+j+N]=i +((i+j) mod M)*N.* (Col. 7, lines 12-64).

Claims 2 and 11:

Lee teaches second and third diagonal interleavings include a process for permuting an input information bit sequence expressed in an MxN matrix and enable input data to be interleaved (calculating an intra-row permutation pattern using the increment incr(j)...) . Lee further teaches diagonal interleaving addresses are operated by:

*for (j=0; j<M; j++) for (i=0; i<N, i++) new addr[i+j+N]=i+(M-1-(i+j) mod M)*N (2)*

where and i and j increment frame location (using the intra-row permutation pattern increment arrangement value incr(j)) and

in the third diagonal interleaving, the diagonal interleaving controller 517 can be implemented by:

*for (j=0; j<M; j++) for (i=0; i<N; i++) new addr[i+j+N]=i +((i+j) mod M)*N.* (Col. 7, lines 12-64). Lee also teaches a diagonal interleaving table 513 (an intra-row permutation pattern storage arrangement device for storing intermediate data) stores the numbers M and N of columns and rows in a matrix allowing optimum diagonal interleaving characteristics with respect to frame size during diagonal interleaving, essentially storing measured MxN values (intermediate data) which enable optimum diagonal interleaving of information bits with a variable frame size. (Col. 5, lines 12-16). Lee further teaches a diagonal interleaving controller 517 receives the MxN value from the diagonal interleaving table 513 and generates a read address for interleaving the information bits in a designated interleaving method. (a final address generator for calculating an address of finally interleaved data).

Claim 3:

Lee teaches a register 511 stores a frame size signal and an interleaver type signal received from a system controller, as well as, a diagonal interleaving table 513 stores the numbers M and N of columns and rows in a matrix allowing optimum diagonal interleaving characteristics with respect to frame size during diagonal interleaving (register updates and registers parameters used to calculate inter-row/intra-row permutation pattern of the input data to be interleaved). Lee also teaches a

diagonal interleaving controller 517 receives the MxN value from the diagonal interleaving table 513 and generates a read address for interleaving the information bits in a designated interleaving method (provides the parameters to an intra-row permutation pattern generator of the address calculator). (Col. 5, lines 12-26).

Claim 5:

Lee teaches deinterleaving is implemented in an order reverse to that of interleaving input data (an inter-row inverse permutation pattern). (Col. 8, lines 5, 6).

Claims 9 and 12:

Lee teaches a memory 523 (data storage device) receives the information bits sequentially and outputs the information bits stored at the read address received from the multiplexer 521 in an interleaved order. (Col. 5, lines 43-46).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 4 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (US-6289486), hereinafter Lee, in view of Li et al. (US-6543013), hereinafter Li.

Claim 4:

"a parameter K indicating a number of input data bits"

Lee teaches a register 511 stores a frame size signal *k* and an interleaver type signal. (Col. 5, lines 12, 13, col. 6, lines 15 and 16)

"a parameter R indicating a number of rows of the input data; a parameter C indicating a number of columns of the input data"

Lee teaches a diagonal interleaving table 513 stores the numbers *M* and *N* of columns and rows in a matrix allowing optimum diagonal interleaving characteristics with respect to frame size during diagonal interleaving. (Col. 5, lines 15, 16).

"a parameter TypeD indicating an exceptional process request signal"

Lee teaches a register 511 stores a frame size signal *k* and an interleaver type signal. (Col. 5, lines 12, 13).

"a parameter μ indicating a primitive root; a parameter p indicating a prime number"

Lee does not explicitly teach a parameter μ indicating a primitive root and a parameter *p* indicating a prime number. However, Li teaches the interleaver includes a storage area containing an array large enough to store the largest expected data frame. Li also teaches a frame of size L elements to be interleaved is stored in $N_r^{(l)}$ rows and $N_c^{(l)}$ columns of the array, where $N_r^{(l)}$ is a predetermined integer and $N_c^{(l)}$ is a prime number which satisfy the inequality. Li further teaches the intra-row permutation uses a special root called the primitive root α_p of prime P_l to construct the set of roots α_j by using a reduced residual system. (Col. 2, lines 22-27, Col. 3, lines 30-40). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lee's interleaver use Li's reduced residual system. The artisan would have been

motivated to do so because the advantage of using Li's special reduced system is to add additional constraints on the intra-row permutation roots to simplify the search computing for the parameter optimization.

Claim 7:

Lee does not explicitly teach an equation to calculate the increment arrangement value incr(j). However, Lee does teach diagonal interleaving addresses are operated by: *for (j=0; j<M; j++) for (i=0; i<N, i++) new addr[i+j+N]=i+(M-1-(i+j) mod M)*N* where and i and j increment frame location. (Col. 7, lines 24-30). Li teaches the calculation of consecutive prime numbers (increment arrangement value) with the following equation:

$$c_l(i)=[\alpha_p^{p(1)} \times c_l(i-1)] \bmod P_l$$

(Col. 3, lines 19-67). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lee's interleaver use Li's reduced residual system. The artisan would have been motivated to do so because the advantage of using Li's special reduced system is to add additional constraints on the intra-row permutation roots to simplify the search computing for the parameter optimization.

Allowable Subject Matter

The following is an Examiner's Statement of Reasons for Allowance:

The prior arts of record teach an interleaver for a turbo encoder with a register for updating and registering a plurality of parameters for setting an operating condition of the interleaver. The prior arts of record also teach an address calculator for generating a

finally interleaved address using an inter-row permutation pattern, an intra-row permutation pattern increment arrangement value and an intra-row permutation basic sequence provided from the register. The prior arts of record further teach a data storage device for storing data input to the turbo encoder and outputting data corresponding to the address generated by the address calculator.; Lee et al. (US-6289486) is one example of such prior arts. The prior arts of record, however, fail to teach, singly or in combination, an intra-row permutation pattern generator which comprises the details disclosed in claim 6, namely, a first adder and a second adder, a first multiplexer, a sign detector connected to the second adder and the first multiplexer, a second multiplexer.

Any comments considered necessary by applicant must be submitted no later than the payment of the Issue Fee and, to avoid processing delays, should preferably accompany the Issue Fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Tong et al. (US-6732316)

Tong teaches turbo encoder and interleaver system, sequentially writing of data into a storage memory, an address calculator (combiner 62), column

and row permutation, and a register for storing operating parameters (FIFO memory 68). (Claims 1, 9, 10 and 12).

b. Suda et al. (US-6553516)

Suda teaches a turbo encoder and interleaver, intra-permutation tables with prime numbers.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (703) 305-8915. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John J. Tabone, Jr.
Examiner
Art Unit 2133

CHRISTINE T. TU
Primary Examiner